In the Claims:

Please cancel claims 1-30 and 32. Please amend claims 31-33, 35, 37, 38 and 45. The claims are as follows:

1 - 30 (Canceled)

31. (Currently Amended) A semiconductor structure, comprising:

an inductor having a top surface, a bottom surface and sidewalls, a lower portion of said inductor extending into but not completely through a single dielectric layer on a semiconductor substrate and an upper portion of said inductor extending above said dielectric layer, said lower portion of said inductor comprising a conductive liner and a core conductor and said upper portion of said inductor consisting of said core conductor; and

means to electrically contact said inductor.

32. (Canceled)

33. (Currently Amended) [[The]] A structure ~~of claim 32~~, comprising:

an inductor having a top surface, a bottom surface and sidewalls, a lower portion of said inductor extending into but not completely through a single dielectric layer on a semiconductor substrate and an upper portion of said inductor extending above said dielectric layer, said lower portion of said inductor comprising a conductive liner and a core conductor and said upper portion of said inductor consists of said core conductor, ~~wherein~~ said core conductor [[is]] comprising Cu and said liner ~~comprises~~ comprising a dual layer of TaN and Ta.

34. (Currently Amended) The structure of claim [[32]] 31, wherein said upper portion further comprises a conductive passivation layer on a top surface and sidewalls of said upper portion of said inductor.

35. (Currently Amended) [[The]] A structure ~~of claim 34~~, comprising:

an inductor having a top surface, a bottom surface and sidewalls, a lower portion of said inductor extending into but not completely through a single dielectric layer on a semiconductor substrate and an upper portion of said inductor extending above said dielectric layer, said lower portion of said inductor comprising a conductive liner and a core conductor and said upper portion of said inductor consisting of said core conductor; and

a conductive passivation layer on a top surface and sidewalls of said upper portion of said inductor, ~~wherein~~ said passivation layer ~~comprises~~ comprising a layer of Ni or a layer of Au over a layer of Ni.

36. (Original) The structure of claim 31, wherein said inductor has a height defined by said sidewalls of greater than about 5 microns.

37. (Currently Amended) [[The]] A structure ~~of claim 31~~, comprising:

an inductor having a top surface, a bottom surface and sidewalls, a lower portion of said inductor extending into but not completely through a single dielectric layer on a semiconductor substrate and an upper portion of said inductor extending above said dielectric layer, ~~wherein~~ said lower portion ~~extends~~ extending a distance of less than 3 microns into said dielectric layer.

38. (Currently Amended) [[The]] A structure ~~of claim 31~~, comprising:

an inductor having a top surface, a bottom surface and sidewalls, a lower portion of said inductor extending into but not completely through a single dielectric layer on a semiconductor substrate and an upper portion of said inductor extending above said dielectric layer; and

wherein ~~said means for contacting said inductor includes~~ integral vias extending from said bottom of said inductor through said dielectric layer and electrically contacting pass through metallurgy in said substrate.

39. (Original) The structure of claim 38, wherein said top surface of said inductor over said vias is closer to a top surface of said dielectric layer than portions of said top surface of said inductor not over said vias.

40. (Original) The structure of claim 31, wherein said inductor extends parallel to a top surface of said dielectric layer in a spiral coil.

41. (Original) The structure of claim 40, wherein said inductor is about 2 to 30 microns wide and adjacent coils of said spiral coil are spaced apart about 2 to 20 microns.

42. (Original) The structure of claim 31, wherein said inductor has an inductance of greater than about 0.5 nH.

43. (Original) The structure of claim 31, wherein said inductor has a Q factor of greater than about 25.

44. (Original) The structure of claim 31, wherein said inductor has a Q factor of greater than about 40.

45. (Currently Amended) [[The]] A structure ~~of claim 31~~, comprising:

an inductor having a top surface, a bottom surface and sidewalls, a lower portion of said inductor extending into but not completely through a single dielectric layer on a semiconductor substrate and an upper portion of said inductor extending above said dielectric layer;

means to electrically contact said inductor; and

a contact pad comprising a via formed in said dielectric layer, said via exposing at least a portion of an I/O terminal pad in said substrate, sidewalls of said via and at least a portion of said I/O terminal pad covered with a passivation layer over a conformal seed layer over a conductive liner.

46. (Original) The structure of claim 45, wherein said conductive liner comprises a dual layer of TaN and Ta, said seed layer comprises Cu and said passivation layer comprises a layer of Ni or a layer of Au over a layer of Ni.

47. (Original) The structure of claim 46, further including an Al or Au wire conductively bonded to said contact pad.

48. (Original) The structure of claim 46 further including a layer of pad limiting metallurgy on said passivation layer and a solder ball on said pad limiting metallurgy.

49. (Original) The structure of claim 48, wherein said pad limiting metallurgy comprises one or more layers selected from the group consisting of Cr layers, CrCu layers, Au layers, Cu layers and TiW layers and said solder ball comprises Pb or Pb/Sn alloy.

50. (Original) The structure of claim 45, wherein said top surface of said inductor is in a different plane than a top surface of said contact pad.

51. (Original) The structure of claim 45, wherein a top surface of said inductor is higher than said top surface of said contact pad relative to a top surface of said dielectric layer.

52. (Original) The structure of claim 31, further including:

an I/O terminal pad formed in said substrate; and

a raised contact pad in electrical contact with said I/O terminal pad, said raised contact pad having a top surface, a bottom surface and sidewalls, a lower portion of said inductor extending said fixed distance into said dielectric layer formed on a semiconductor substrate and an upper portion extending above said dielectric layer.

53. (Original) The structure of claim 52, wherein said lower portion of said raised contact pad comprises a conductive liner and a core conductor and said upper portion of said raised contact pad comprises said core conductor.

54. (Original) The structure of claim 53, wherein said core conductor is Cu and said liner comprises a dual layer of TaN and Ta.

55. (Original) The structure of claim 53, wherein said upper portion further comprises a conductive passivation layer on said top surface and sidewalls of said upper portion of said raised contact pad.

56. (Original) The structure of claim 55, wherein said passivation layer comprises layer of Ni or a layer of Au over a layer of Ni.

57. (Original) The structure of claim 56, further including an Al or Au wire conductively bonded to said raised contact pad

58. (Original) The structure of claim 56 further including a layer of pad limiting metallurgy on said passivation layer and a solder ball on said pad limiting metallurgy.

59. (Original) The structure of claim 58, wherein said pad limiting metallurgy comprises one or more layers selected from the group consisting of Cr layers, CrCu layers, Au layers, Cu layers and TiW layers and said solder ball comprises Pb or Pb/Sn alloy.

60. (Original) The structure of claim 52, wherein said top surface of said inductor is in a different plane than a top surface of said raised contact pad.

61. (Original) The structure of claim 52, wherein a top surface of said inductor is higher than said top surface of said raised contact pad relative to a top surface of said dielectric layer.